METHOD FOR SUPPORTING MULTIPLE DEVICES ON A HIGH SPEED PHYSICAL LINK

BACKGROUND OF THE INVENTION

There are numerous applications for embedded microprocessor devices. These applications may include various technologies for cellular telephones, notebook computers, handheld computers, personal digital assistants, automobiles, appliances and other consumer products. For example, a cellular phone may have an embedded general applications processor and a baseband processor. Typically, the applications processor may manage database applications while the baseband processor may support a communications platform such as General Packet Radio Service (GPRS) or Code Division Multiple Access (CDMA).

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The number of microprocessors that are being embedded into devices, particularly handheld devices, is increasing to provide customers with additional features. These new features have increased the types and amounts of data embedded processors exchange with other microprocessors, peripherals and/or external servers. For example, embedded microprocessors now exchange everything from command and control data to large databases and streaming data for voice and video communications.

In the past, if there was a need for inter-processor communications, these communications could be accomplished through a low-speed physical link, such as a serial interface, which may have limited quality of service (QoS) and data reliability management. However, today's designers are integrating new features into handheld devices such as CMOS digital imaging, World Wide Web (WWW) access and multimedia processing. In addition, handheld devices are also supporting more recent communications platforms such as Wideband Code Division Multiple Access (WCDMA), IEEE 802.11, Bluetooth® and the like for next generation wireless applications. This expansion of capabilities has led to the emergence of handheld devices that are structured more like personal computers. For example, these devices might include an applications subsystem for implementing various

database and multimedia applications and then separate communications subsystems for implementing wireless communications.

Separate processor subsystems have necessitated an increased focus by circuit designers on high-speed processor to processor communications. Recently, particular attention has been paid to providing a high-speed, reliable standard for a communications interface between an embedded general purpose applications processor and a baseband processor. One example of a high-speed processor to processor communications interface is Intel® Corporation's Multiple Scalable Link® (MSL) technology. Factors considered for an inter-processor communications standard may include high inter-processor data transmission rates, scalability for increasing bandwidth, QoS, security, and the elimination of data exchange bottlenecks. Unlike the typical personal computer, however, these devices have to be designed with severe packaging and power consumption constraints in mind.

BRIEF DESCRIPTION OF DRAWINGS

Embodiments of the present invention may be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

- Fig. 1 illustrates an inter-processor communications link.
- Fig. 2 illustrates an inter-processor communications link according to one embodiment of the present invention.
 - Fig. 3 shows a flowchart illustrating a possible mode of operation of an embodiment of the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention numerous specific details may be set forth in order to provide a thorough understanding of embodiments of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices may be shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

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Reference in the specification to "one embodiment" or "an embodiment" may mean that a particular feature, structure, or characteristic described in connection with the embodiment may be included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

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The apparatuses presented herein are not inherently related to any particular device, circuit or other apparatus. Various general purpose devices or circuits may be used with the apparatuses in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus or device to use in conjunction with the apparatuses. In addition, embodiments of the present invention may not be described with reference to any particular device, circuit or other apparatus. It will be appreciated that a variety of devices, circuits or other apparatuses may be used in conjunction with the apparatuses as described herein.

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Referring now to Fig. 1, an illustration of a system 100 for multi-point communications is presented. Device '0' 102 may be an embedded processor device which may be, for example, a general applications processor for a radio telecommunications device, such as, but not limited to, a radio telephone or a personal digital assistant (PDA). In one embodiment, a general applications processor may be focused on running database applications such as World Wide Web surfing or multimedia processing. Device '1'through device 'N', 104, 106 and 108 respectively, may be embedded processor devices. These embedded devices may include a general applications processor device, a baseband

processor device or other general or dedicated processor devices. For example, the system 100 may represent a baseband processor to applications processor interface for a "smart" radio telephone medium. The smart telephone may include separate applications and communications subsystems, wherein, for example, the applications subsystem might be represented by device '0' 102 and various communications subsystems may by represented by devices '1'-'N', 104 to 108 respectively. In one embodiment, the communications subsystems may include multiple baseband processors such as CDMA processors, WCDMA processors, Bluetooth processors, IEEE 802.11 processors and/or other baseband processor devices. In one embodiment, the communications subsystems may include processors for multiple cellular basebands for supporting various cellular transmission standards. In another embodiment, the devices '1'-'N', 104 to 108 respectively, may also comprise processors for hardware accelerator applications, audio code/decode (CODEC) applications, digital signal processing and/or other applications.

In one embodiment, the multi-point, inter-device communications link 110 may be a data link between a plurality of applications and/or communications subsystems. For example, the link 110 may be a dedicated and optimized high speed interface that allows for multi-point data transmissions between a plurality of embedded applications processor devices. One inter-device communications link 110 that may be suitable for performing the functions described herein is the Intel® Corporation's Multiple Scalable Link® (MSL) technology, however, this link is not limited to such inter-device communications link. As such, other inter-device communications links capable of, for example, one megabit/second or greater data rates and for providing a common, multi-point interface for communicating between embedded applications processors, may be suitable for performing the functions herein.

Fig. 2 illustrates a multi-point, inter-device communications link 110 according to one embodiment of the present invention. In one embodiment, device '0' 102 may represent an applications processor. For example, device '0' 102 may initially control the flow of data on the link 110 between the embedded devices or may be operable to configure the other embedded devices. The clock pin 200 may be activated to control the timing for a data transmission on the link 110. For example, in a handheld device where power conservation

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may be an issue, the clock 200 may be driven only when data is being transferred on the link 110. Strobe 202 may be activated to frame a data packet so as to tell a receiving device when a packet is coming and the channel that it will be transmitted over. For example, when the strobe 202 is activated, the receiving device may know to look at the data pins 206, which may tell the receiving device what channel the data may be being transmitted on. For a multi-point communications link 110 for example, the activation of the strobe 202 followed by a device identification indicated by the data pins 206 may be used to transmit which device out of the plurality of embedded devices may be targeted to receive data.

The wait pin 204 may be a data flow control mechanism which the receiving device may assert when it may not accept any more data, thus it may prevent an overrun condition. When the wait pin 204 goes inactive, the sending device may know that it may resume transmitting data to the receiving device. The wait pin 204 may also be used as an acknowledgement signal for a device requesting to transmit data on the link 110, as described below.

The link request (LReq) pin 208 may be an arbitration pin that may be shared between the plurality of embedded devices operable to utilize the link 110. Packaging constraints in a handheld device, for example, may make it advantageous to reduce pin count by multiplexing the LReq pin 208 between the plurality of embedded devices. In another embodiment, each device operable to utilize the link 110 to transmit data may have a dedicated LReq pin 208.

In one embodiment, in order to avoid data corruption, only one device may be permitted to transmit data on the link 110 at a time. Therefore, when a device activates the LReq pin 208, an arbitration may begin to determine the requesting device and may handoff permission to transmit data on the link 110 from the controlling device to the requesting device.

Fig. 3 illustrates a flowchart 300 representing one embodiment of the present invention. In operation, after a start up phase in which a device having permission to transmit data on the link 110 may be established, at 302, a device that may wish to transmit

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data on the link, or a requesting device, may activate the LReq pin 208. When the LReq pin 208 is activated, the device permitted to transmit on the link, or the controlling device (e.g., sometimes referred to as a "controller" or an "embedded controlling device"), may receive the activated LReq signal at 304 and may begin an arbitration cycle. Alternatively, the controlling device may determine that it does not want to relinquish control of the link 110, for example, if it is still in the process of transmitting data. The controlling device may wait until it is finished transmitting data to begin an arbitration cycle. In one embodiment, the requesting device may not have to reactivate the LReq pin 208 if the controlling device does not immediately begin an arbitration cycle. The LReq pin 208 may stay activated until it is acknowledged by the controlling device.

When the controlling device determines that it is ready to transfer permission to transmit data on the link to another device at 306, the controlling device may address the plurality of embedded devices and may determine which device activated the LReq pin 208 for control of the link 110 at 308. At 310, the controlling device may address each of the plurality of embedded devices and may determine which device activated the LReq pin 208 until it receives an acknowledgement signal. In one embodiment, the controlling device may address the plurality of embedded devices utilizing a round-robin method. For example, if device '1' 104 is the controlling device, it may address device '2' 106 first by activating the strobe pin 202 followed by the device ID for device '2' 106. If device '2' 106 is the requesting device, it may send a confirmation signal to the controlling device. In one embodiment, the requesting device may activate the wait pin 204 when it is addressed by the controlling device as a confirmation signal. If device '2' 106 is not the requesting device, the controlling device may determine whether there are additional embedded devices at 312 and may then address each one in turn 308 and may determine if the addressed device is the requested device. For example, if device '2' 106 is not the requesting device, the controlling device may address a device '3', '4' (not shown) and so on until either the requesting device is found or there are no more devices to address, in which case the controlling device may maintain permission to transmit data across the link 110 at 316. Alternatively, other methods for determining the requesting device, which may be implemented by hardware, software, firmware or any combination thereof, may be implemented by the controlling device. Other methods, including, but not limited to

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methods which guarantee priority for certain devices when they are the requesting device will be familiar to one who is skilled in the art.

When the requesting device is found by the controlling device, the controlling device may handoff the permission to transmit data on the link 110 to the requesting device at 314. Again, techniques for transferring the control of the data link should also be well known to one skilled in the art. One skilled in the art will find that several handoff techniques may be adequate and equally suitable for implementing the features of the present invention described herein. When the handoff is complete, the new controlling device may be permitted to transmit data on the link 110 at 316.

It should be appreciated that while the present invention may be implemented in many types of electronic devices including radio telephones, personal computers, server computers, hand-held or laptop devices, multiprocessor systems, microprocessor-based systems, set top boxes, programmable consumer electronics, network PCs, minicomputers, mainframe computers and distributed computing environments that include any of the above systems or devices, an exemplary environment for the implementation of the present invention is on a serial communications link that electrically connects embedded CMOS applications microprocessors.

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The present invention has been described in relation to particular embodiments, which are intended in all respects to be illustrative rather than restrictive. Alternate embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly, the scope of the present invention is to be limited only by the claims below.